DATA SHEET

BGB100
0 dBm TrueBlue radio module

Preliminary specification

2002 Jan 03

Philips
Semiconductors

PHILIPS

0 dBm TrueBlue radio module BGB100

FEATURES

- Plug-and-play Bluetooth class 2 radio module, needs only external antenna and reference clock
- Small dimensions (12.25 x 9.8 x 1.9 mm)
- Fully compliant to Bluetooth Radio Specification v1.1
- High sensitivity (typical –80 dBm)
- Advanced DC offset compensation for improved reception quality
- RSSI with high dynamic range
- Simple interfacing to baseband controller, control by 3-wire serial bus
- Internal shielding for better EMI (Electro Magnetic Interference) immunity.

APPLICATIONS

Bluetooth transceivers in:

- Cellular phones
- Laptop computers
- Personal digital assistants
- Consumer applications.

DESCRIPTION

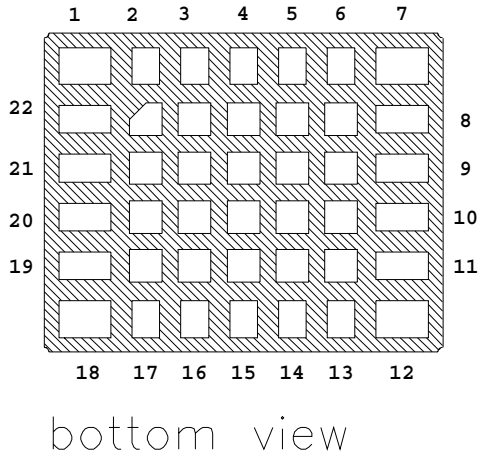
The BGB100 TrueBlue Bluetooth radio module is a short-range radio transceiver for wireless links operating in the globally available ISM band, between 2402 and 2480 MHz. It is composed of a fully integrated, state-of-the-art near-zero-IF transceiver chip, an antenna filter for out-of-band blocking performance, a TX/RX switch, TX and RX baluns, the VCO resonator and a basic amount of supply decoupling. The device is a “Plug-and Play” module that needs no external components for proper operation. Robust design allows for untrimmed components, giving a cost-optimized solution.
Demodulation is done in open-loop mode to reduce the effects of reference frequency breakthrough on reception quality. An advanced offset compensation circuit compensates for VCO drift and RF frequency errors during open-loop demodulation, under control by the baseband processor.
The circuit is integrated on a ceramic substrate. It is connected to the main PCB through a LGA (Land Grid Array). The RF port has a normalized 50 Ω impedance and can be connected directly to an external antenna, with a 50 Ω transmission line.

The interfacing to the baseband processor is very simple, which leads to a low-power solution. Control of the module operating mode is done through a 3-wire serial bus and one additional control signal.
TX and RX data I/O lines are analogue-mode interfaces. A high-dynamic range RSSI output allows near-instantaneous assessment of radio link quality.
Frequency selection is done internally by a conventional synthesizer. It is controlled by the same serial 3-wire bus. The synthesizer accepts reference frequencies of 12, 13, 16 and 26 MHz. This reference frequency should be supplied by an external source. This can be a dedicated (temperature compensated) crystal oscillator or be part of the baseband controller.
The circuit is designed to operate from 3.0 V nominal supplies. Separate ground connections are provided for reduced parasitic coupling between different stages of the circuit. There is a basic amount of RF supply decoupling incorporated into the circuit.
The envelope is a leadless SOT649A package with a plastic cap.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING

PIN	NAME	DESCRIPTION
1,4,7,9, 12,17,18, 19,20,22, 23	GND	ground
2	V_{S1}	supply (for VCO, buffer and synthesizer)
3	T_GFSK	transmit data input
5	R_DATA	received data output
6	RSSI	received signal strength indicator
8	REFCLK	reference clock input
10	S_DATA	3-wire bus data input
11	S_EN	3-wire bus enable input
13	S_CLK	3-wire bus clock input
14	V_{S2}	supply (for RX part, TX part)
15	DCXCTR	DC extractor control signal
16	NC	not connected
21	ANT	antenna input/output



Pin 23 represents the inner 5 x 4 = 20 LGA pads

Fig.1 Simplified outline

BLOCK DIAGRAM

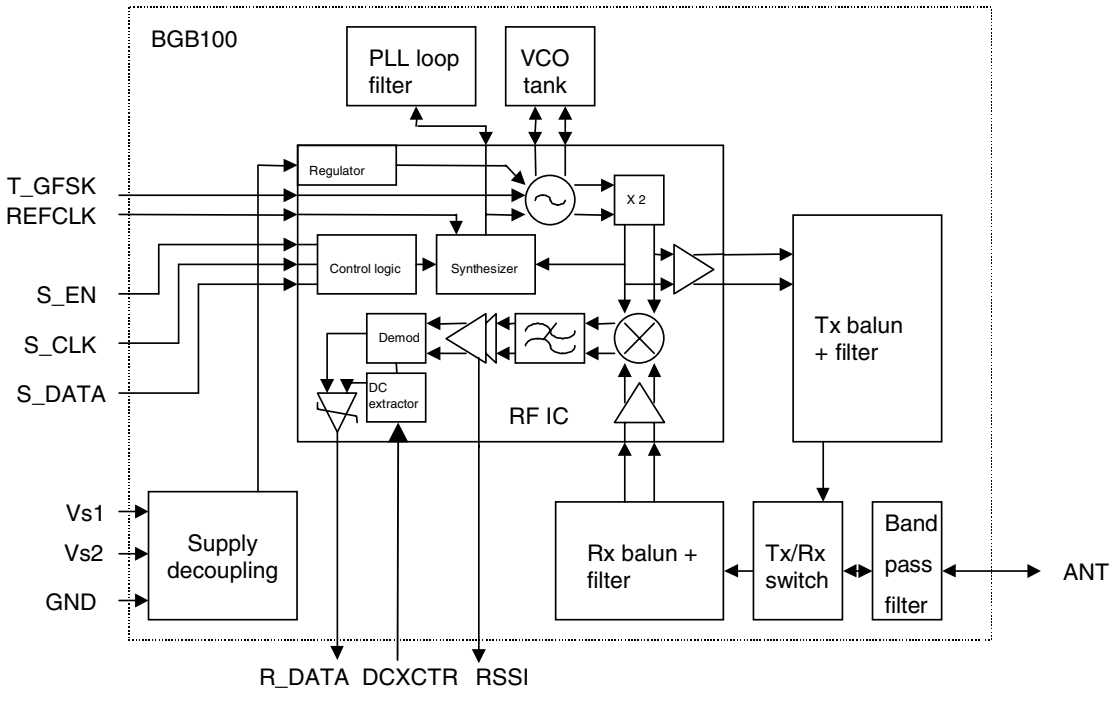


Fig.2 Block diagram.

QUICK REFERENCE DATA

V_S = 3.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_S	nominal supply voltage		2.8	3	3.6	V
$I_{S1} + I_{S2}$	total supply current	during RX guard space	–	25	–	mA
		during demodulation	–	60	72	mA
		during TX guard space	–	36	–	mA
		during transmission	–	34	40	mA
		in power-down mode	–	10	60	μA
Sens	receiver sensitivity	BER = 0.1 % under standard conditions	–	–80	–73	dBm
P_{out}	output power	at nominal settings	–4	–1.5	+4	dBm
f_0	RF frequency		2402	–	2480	MHz
f_{ref}	reference input frequency		12	–	26	MHz
T_{amb}	operating ambient temperature(1)		–10	–	55	°C

Note

1. In combination with the adaptive temperature-compensation scheme provided by the baseband processor

FUNCTIONAL DESCRIPTION

Control

The BGB100 TrueBlue Bluetooth Radio Module is controlled by a baseband processor via the serial 3-wire bus. These 3 wires are data (S_DATA), clock (S_CLK) and enable (S_EN). Data sent to the device is loaded in bursts framed by S_EN. Data and clock (S_DATA and S_CLK) signals are ignored until S_EN goes low. The programmed information is read directly into the internal registers when S_EN goes high. S_DATA and S_EN should be stable around the rising edges of S_CLK. There are internal pull-down resistors on all these three pins.

Only the last 32 bits serially clocked into the device are retained within the register. Additional (leading) bits are ignored, and no check is made on the number of bits received. The data format is shown in table 1. The first data bit entered is b31, the last one b0.

The S_EN high-to-low transition also controls the opening of the PLL. A short S_EN high pulse at the end of a time slot, either TX or RX, serves to reset and power-down the IC. This can be omitted, at the cost of extra power consumption.

In addition to the 3-wire serial bus, there is one control signal used for accurate timing of functions within the IC, under control by the baseband processor. This is the DCXCTR signal, to control (in RX mode) the three subsequent operating modes of the DC compensation circuit: coarse offset estimation during the early part of the Access Code, accurate offset estimation during the Barker sequence and the trailer, retention of the offset information during the payload.

Transmit mode

The BGB100 TrueBlue Bluetooth Radio Module contains a fully integrated transmitter function. The RF channel frequency is selected in a conventional synthesizer, which is controlled via the serial 3-wire bus. The VCO is directly modulated by the signal present on the T_GFSK connection. The Gaussian filtering should therefore be performed externally. The DC bias voltage for this pin should already be present during the S_EN programming pulse, so that the PLL can correct for possible frequency errors that might otherwise occur. Also in RX mode, this pin should be connected to a well-defined and stable DC voltage. The robust design of the VCO makes it unnecessary to trim its freerunning frequency. This leads to a lower component cost. A carefully designed PLL loop filter keeps frequency drift during open-loop modulation down to a very low value.

The output stage of the transmit chain active part is balanced, for reduced spurious emissions (EMC). It is connected through a balun (balanced-to-unbalanced) circuit to the TX/RX switch. This switch is controlled by internal logic circuits in the active die. The balun circuit has built-in selectivity, to further reduce out-of-band spurious emissions.

Receive mode

Also the receiver functionality is fully integrated. It is a near-zero-IF (1 MHz) architecture with active image rejection. The sensitive RX input of the active die is a balanced configuration, in order to reduce unwanted (spurious) responses. The balun structure to convert from unbalanced to balanced signals has built-in selectivity. This suppresses GSM-900 frequencies by more than 40 dB. For better immunity to DCS, DECT, GSM-1800 and W_CDMA signals, an extra band-pass filter has been included.

The synthesizer PLL may be switched off during demodulation. This reduces the effects that reference frequency breakthrough may have on receiver sensitivity and adjacent channel selectivity, and also reduces the power consumption. The demodulator contains an advanced DC offset compensation circuit. This reduces the effects of frequency mismatch between (remote) transmitter and receiver. These may be caused by differences in reference frequency, but also by frequency drift during open-loop modulation and demodulation.

Because the VCO is directly modulated by the signal present at the T_GFSK pin, this pin should be connected to a well-defined and stable DC bias voltage, also when in RX mode. Moreover, this bias voltage should already be present during the S_EN programming pulse. In this way, the PLL can correct for possible frequency offsets that might otherwise occur.

The demodulated RF signal is compared against a reference (slicer) value and then output. This reference voltage is derived from the demodulated output signal itself, by the DC extractor circuit. It operates in three subsequent phases, controlled by the DCXCTR signal:

- In the first phase, during the preamble and the early part of the Acess Code, a Min/Max detector provides a crude but fast estimate of the required DC voltage. The DCXCTR line should be low during this phase.
- When the DCXCTR line is pulled high, this crude estimate is used as an initial estimate for an integrator circuit that provides an accurate estimate of the required DC voltage. This is the second phase. The DC value obtained is derived from the Barker sequence and the trailer, which together make up the final 10 bits of the Acess Code. The DCXCTR line should be pulled high 20 μs before the trailer sequence is expected to end (there is a ±10 μs timing uncertainty between the expected and the actual end of the trailer sequence).
- Exactly at the end of the trailer, the DCXCTR line must be pulled low again. The device now enters the third phase, during which the estimate of the offset voltage that was obtained during phases one and two is retained. A small and slow variation to compensate carrier frequency drift can still be tracked.

An RSSI output with a high dynamic range of more than 50 dB provides near-instantaneous information on the quality of the signal received.

Due to the IF frequency at 1 MHz, in RX mode the VCO frequency should be 1 MHz higher than the channel frequency. This should be taken care of by the baseband controller.

Power-down mode

In Power-down mode, current consumption is reduced to below 60 μA. The 3-wire bus inputs present a high-ohmic resistance to ground.

Table 1 Bit allocation

REGISTER BIT ALLOCATION[1]																
Data field																
FIRST IN																
b31	b30	b29	b28	b20	b26 [2]	b25 [2]	b24 [2]	b23 [2]	b22	b21	b20	b19	b18	b17	b16	see below
0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	0	
LAST IN																
see above	b15	b14	b13	b12	b11	b10	b9	b8	b7 to b0 [7]							
	0	0	ref1 [3]	ref0 [3]	pwr1 [4]	pwr0 [4]	pll [5]	trx [6]	main divider programming [8]							

Notes

1. In normal operation, 32 bits are programmed into the register.
2. bits b26 to b23 can be used for adaptive temperature compensation by the baseband.
3. ref: bits ‘ref1’ and ‘ref0’ define the reference frequency (see Table 3).
4. pwr: bits ‘pwr1’ and ‘pwr0’ define the the typical output power (see Table 4).
5. trx: bit ‘trx’ = 1 forces the IC into RX mode.
6. pll: bit ‘pll’ = 1 forces the synthesizer PLL to remain on during the entire (TX or RX) slot.
7. Bit b7 is the MSB of the frequency control word composed of (b7, b6, b5, b4, b3, b2, b1 and b0).
8. The VCO frequency is equal to 2304 + d[b7:b0] (see Table 2).

Table 2 Channel frequency programming examples

b7	b6	b5	b4	b3	b2	b1	b0	MAIN DIVIDER RATIO	SYNTHESIZED FREQUENCY (MHz)	CHANNEL FREQUENCY
Binary equivalent of n								2304 + n	1.0 × (2304 +n)	
0	1	1	0	0	0	1	0	2402	2402	TX channel 1
0	1	1	0	0	0	1	1	2403	2403	RX channel 1 TX channel 2
1	0	1	1	0	0	0	0	2480	2480	RX channel 78 TX channel 79
1	0	1	1	0	0	0	1	2481	2481	RX channel 79

Table 3 Reference frequency programming

b13	b12	REFERENCE DIVIDER RATIO	REFERENCE INPUT FREQUENCY
0	0	12	12 MHz
0	1	16	16 MHz
1	0	13	13 MHz
1	1	26	26 MHz

Table 4 Typical output programming

b11	b10	TYPICAL OUTPUT POWER
0	0	−4.5 dBm
0	1	−1.5 dBm (nominal value)
1	0	1.5 dBm
1	1	3.5 dBm

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{S1}, V_{S2}	supply voltage		−0.3	3.6	V
	input control pin voltage		−0.3	V_S	V
ΔGND	difference in ground supply voltage between ground pins		−	0.01	V
P_{tot}	total power dissipation		−	tbd	W
P_D	drive power at receiver input		−	0	dBm
T_{stg}	storage temperature		−55	85	°C
T_j	junction temperature		−	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	tbd	K/W

SPURIOUS EMISSIONS

The conducted and radiated out-of-band spurious emissions in all operating modes are fully compliant with the Regulatory Requirement FCC Part 15.247,C and ETS 300 328 (subclause 5.2.4.).

ESD PRECAUTIONS

Inputs and outputs are protected against electrostatic discharge (ESD) during handling and mounting. A human-body model (HBM) and a machine model (MM) are used for ESD susceptibility testing. All pins withstands the following threshold voltages:

PARAMETER	METHOD	VALUE	CLASS
ESD threshold voltage	HBM (JESD22-A114-B)	≥3500 V	2
	MM (JESD22-A115-A)	≥300 V	2

CHARACTERISTICS

V_{CC} = 3.0 V;T_{amb} = 25 °C; f_{dev} = 160 kHz; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{S1}, V_{S2}	nominal supply voltage		2.8	3.0	3.6	V
$I_{S1} + I_{S2}$	total supply current	during RX guard space	–	25	–	mA
		during RX (PLL off)	–	60	72	mA
		during TX guard space	–	36	–	mA
		during TX (PLL off)	–	34	40	mA
		power-down mode	–	10	60	μA
Frequency selection						
f_{ref}	reference input frequency			12,13, 16,26		MHz
Δf_{ref}	reference frequency inaccuracy		tbd	–	tbd	ppm
$V_{ref(min)}$	sinusoidal input signal level	RMS value	250	–	500	mV
R_i	input resistance (real part of the input impedance)	at 13MHz	–	2	–	kΩ
C_i	input capacitance (imaginary part of the input impedance)	at 13MHz	–	2.5	–	pF
$\Delta f_{1\ slot}$	carrier drift	over 1 TX slot	–25	0	25	kHz
$\Delta f_{3,\ 5\ slots}$		over 3, 5 TX slots (DM3, DH3, DM5, DH5 packets)	–40	0	40	kHz
ICFT	Initial Carrier Frequency Tolerance		–75	0	75	kHz
t_{PLL}	PLL settling time	across entire band	–	150	200	μs
Transmitter performance						
f_{RF}	RF frequency	over full temperature and supply range	2402	–	2480	MHz
k_{MOD}	VCO modulation gain	from T_GFSK (pad 3) to antenna (pad 21): note 2	–	400	–	kHz/V
P_o	output power	wanted channel; bits b11, b10 = 0, 1	–4	–1.5	4	dBm
$P_{o\ 1\ MHz}$	adjacent channel output power	at 1 MHz offset; measured in 100 kHz bandwidth; referred to wanted channel	–	–	–20	dBc
VSWR	voltage standing wave ratio	normalized to Z_o = 50 Ω	–	1.5	–	
$H_{1,\ VCO}$	VCO frequency feedtrough	referred to wanted output level; f_{RF} = 2450 MHz; f_{VCO} = 1225 MHz	–	tbd	tbd	dBc
$H_{3,\ VCO}$	VCO 3rd harmonic		–	tbd	tbd	dBc
$H_{4,\ VCO}$	VCO 4th harmonic		–	tbd	tbd	dBc
$H_{6,\ VCO}$	VCO 6th harmonic		–	tbd	tbd	dBc

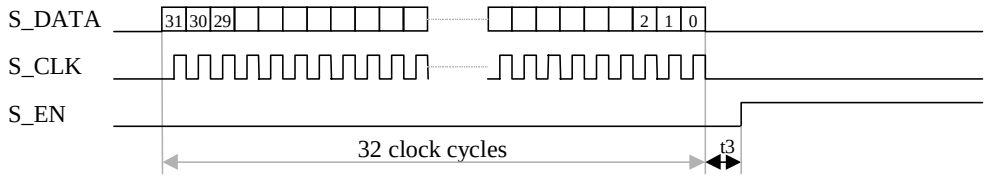
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	out of band spurious emissions (conducted)	30 MHz to 1 GHz	–	tbd	–36	dBm
		1 GHz to 12.75 GHz	–	tbd	–30	dBm
		1.8 GHz to 1.9 GHz	–	tbd	–47	dBm
		5.15 GHz to 5.3 GHz	–	tbd	–47	dBm
Receiver performance						
SENS	sensitivity for BER = 0.1 %	without carrier offset	–	–80	–73	dBm
		with carrier offset up to ±55 kHz under extreme test conditions	–	–	–70	dBm
$P_{i\ max}$	maximum input power in one channel	BER < 0.1 %	–20	–	–	dBm
VSWR	voltage standing wave ratio	normalized to Z_o = 50 Ω	–	1.5	–	
f_{RF}	RF input frequency	over full temperature and supply range	2402	–	2480	MHz
V_{RSSI}	RSSI voltage (monotonic over range –86 dBm to –36 dBm)	P_{in} = –86 dBm	–	0.5	–	V
		P_{in} = –36 dBm	–	1.3	–	V
T_{on}	wake up time from the power up signal to correct RSSI output	No external capacitor on the RSSI pin; R_{load} > tbf kΩ	–	tbd	50	µs
IM_3	intermodulation rejection	wanted signal –64 dBm; Interferers 5 and 10 channels away; BER < 0.1 %	–	25	–	dBc
R_{CO}	co-channel rejection	wanted signal –60dBm; BER < 0.1 %	–14	–11	–	dBc
$R_{C/I\ 1MHz}$	adjacent channel rejection (± 1 MHz)	wanted signal –60dBm; BER < 0.1 %	–4	0	–	dBc
$R_{C/I\ -2MHz}$	bi-adjacent channel rejection (N-2)	wanted signal –60dBm; BER < 0.1 %	30	35	–	dBc
$R_{C/I\ Image}$	rejection at image frequency (N+2)	wanted signal –60dBm; BER < 0.1 %	6	10	–	dBc
$R_{C/I\ Image\ 1MHz}$	rejection at image-adjacent frequency (N+3)	wanted signal –67dBm; BER < 0.1 %	16	20	–	dBc
$R_{C/I\ \geq 3MHz}$	in-band interference rejection ratio, three or more channels away, except (N+3) and spurious response frequencies	wanted signal –67dBm; BER < 0.1 %	40	–	–	dBc
$R_{C/I\ spurious}$	rejection at five spurious response frequencies in the range [2400 MHz to (N–3) or (N+4) to 2480 MHz]	wanted signal –67dBm; BER < 0.1 %	37	40	–	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	out of band blocking	wanted signal –67dBm; CW interferer level				
		range 30 MHz to 2 GHz	–10	–	–	dBm
		range 2 GHz to 2400 MHz	–27	–	–	dBm
		range 2500 MHz to 3 GHz	–27	–	–	dBm
		range 3 GHz to 12.75 GHz	–10	–	–	dBm
		wanted signal –67dBm; GSM modulated signal between 880 and 915 MHz (GSM–900 uplink)	–	tbd	–	dBm
		wanted signal –67dBm; GSM modulated signal between 1800 and 1785 MHz (GSM–1800 uplink)	–	tbd	–	dBm
	spurious emissions	30 MHz to 1 GHz	–	tbd	–36	dBc
		1 GHz to 12.75 GHz	–	tbd	–30	dBc
FTLOrf	LO to RF feedthrough	measured at 2450MHz	–	tbd	–47	dBc
Interface (logic) inputs and outputs; pins S_DATA, S_CLK, S_EN, DCXCTR, R_DATA, T_GFSK						
V_{IH}	HIGH-level input voltage	note 3	1.4	–	V_S	V
V_{IL}	LOW-level input voltage		–	–	0.4	V
I_{bias}	input bias current	HIGH or LOW level	–5	–	5	µA
f_{S_CLKmax}	maximum 3-wire bus frequency	note 4	–	10	–	MHz
t_{S_ENmin}	minimum S_EN pulse duration	to switch off the module: note 3	–	1	–	µs
V_{OH}	HIGH-level output voltage	for R_DATA output	2.1	–	2.4	V
V_{OL}	LOW-level output voltage	for R_DATA output	–0.3	–	0.4	V
$R_{R\_DATA, load}$	real part of the R_DATA load admittance	at 500 kHz	–	tbd	–	Ω
$C_{R\_DATA, load}$	imaginary part of the R_DATA load admittance	at 500 kHz	–	10	30	pF
$V_{T\_GFSK,DC}$	T_GFSK DC voltage	note 2	–	1	–	V
$R_{T\_GFSK,in}$	real part of the T_GFSK input admittance	at 500 kHz	–	tbd	–	Ω
$C_{T\_GSFK, in}$	imaginary part of the T_GFSK input admittance	at 500 kHz	–	tbd	–	pF

Notes

1. The actual VCO frequency is one-half the programmed frequency. It is doubled internally.
2. T_GFSK is DC coupled. The DC voltage must be supplied by the baseband processor.
3. V_{IH} should never exceed 3.6V.
4. See detailed timing information.

TIMING DIAGRAMS



3-wire serial bus timing

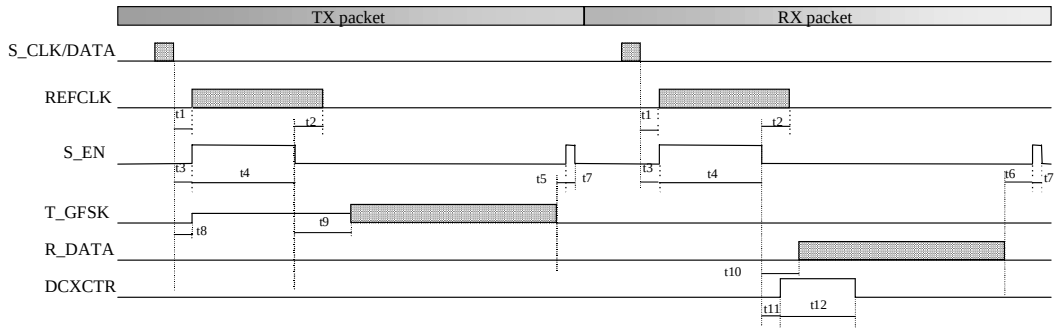


Fig.3 Timing diagram.

Timing Parameters

PARAMETER	DESCRIPTION	CONDITIONS	MIN.	TYP.	UNIT
t1	S_DATA last bit to REFCLK enable		0.1	–	µs
t2	S_EN falling edge to REFCLK disable		–	2	µs
t3	S_DATA last bit to S_EN rising edge		0.1	–	µs
t4	S_EN width	note 1	180	185	µs
t5	T_GFSK last bit to S_EN pulse start		–	2	µs
t6	R_DATA last bit to S_EN pulse start		–	2	µs
t7	S_EN pulse width	note 2	–	2	µs
t8	S_DATA last bit to T_GFSK DC bias	note 3	0.1	–	µs
t9	S_EN falling edge to T_GFSK first data bit		–	2	µs
t10	S_EN falling edge to R_DATA earliest data bit		15	20	µs
t11	S_EN falling edge to DCXCTR high	note 4	–	64	µs
t12	DCXCTR width	note 5	–	20	µs

Notes

1. The S_EN signal going high switches the synthesiser on if preceded by S_DATA / S_CLK activity; the S_EN signal going low disables the synthesizer in order to perform open-loop modulation or demodulation. Simultaneously, it enables the receiver chain in RX mode. The length of the S_EN signal should be long enough for the synthesizer loop to settle.
2. A single short S_EN pulse (without preceding S_DATA / S_CLK activity) serves to power-down the IC. It may be omitted at the cost of increased power consumption. Any subsequent S_EN pulse without preceding S_DATA / S_CLK activity toggles between power-up and power-down states, but brings the module into an undefined power-up state. This mode should be avoided.
3. Because the VCO is directly modulated by the T_GFSK signal, the DC level on this pin should be present early on during the synthesizer settling phase. Also in RX mode, there should be a well-defined and stable DC voltage on this pin.
4. The DCXCTR signal should go high 20 µs before the expected end of the trailer sequence.
5. The DCXCTR signal should go low at the actual end of the trailer sequence. The timing for this transition should be directly derived from the Acess Code detection algorithm inside the baseband processor.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens. A double reflow process is permitted.

Hand soldering is not recommended because of the nature of the contacts.

The maximum allowed temperature is 250 °C for a maximum of 5 seconds.

The maximum ramp-up is 10 °C per second.

The maximum cool-down is 5 °C per second.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

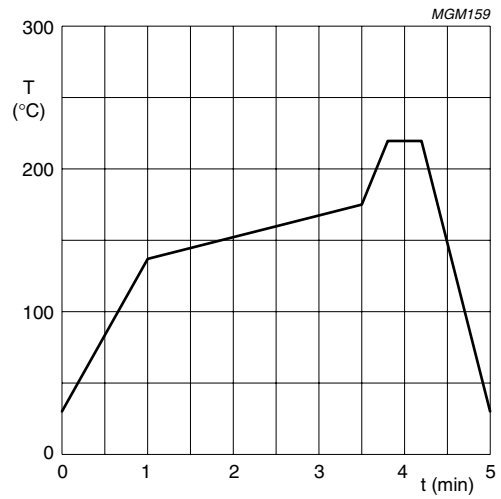


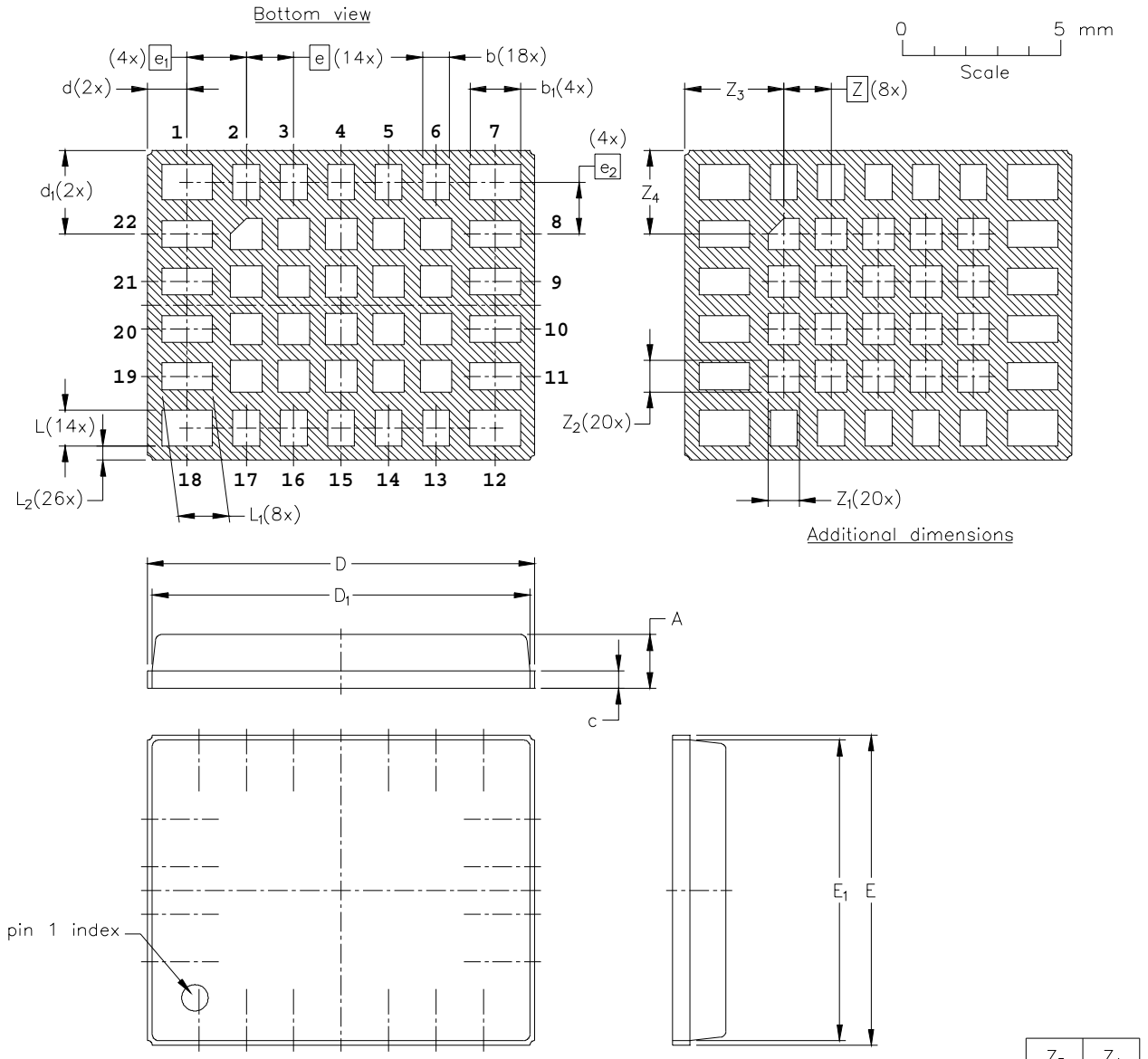
Fig.5 Recommended reflow temperature profile.

Packing

An extended packing / SMD specification can be found in document RNR-T49D-2183.

PACKAGE OUTLINE **SOT649A**

Surface mounted package; plastic cap; 22 terminations



Z_3	Z_4
3.275 2.975	2.8 2.5

UNIT	A	b	b_1	c	D	D_1	d	d_1	E	E_1	e	e_1	e_2	L	L_1	L_2	Z	Z_1	Z_2
mm	1.9 1.7	0.9 0.8	1.65 1.55	0.6 0.5	12.55 11.95	12.05 11.85	1.4 1.1	2.8 2.5	10.1 9.5	9.6 9.4	1.5	1.875	1.64	1.175 1.075	1.65 1.55	0.6 0.3	1.5	1.05 0.95	1.05 0.95

PACKAGE OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT649A PUBLICATION DRAWING					01–10–25

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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SCA73

Printed in The Netherlands budgetnum/ed/pp16 Date of release: 2002 Jan 03 Document order number: 9397 750 09278

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